TESTING HARD-WIRED IP INTERFACE SIGNALS USING A SOFT SCAN CHAIN

ABSTRACT OF THE DISCLOSURE

A set of boundary scan registers are implemented by reconfiguring the functional blocks of a reconfigurable device. This "soft-wired" set of boundary scan registers can be used to test the interface connections between the IP core and the functional blocks of the reconfigurable device. Additionally, the set of boundary scan registers only exists when a testing configuration is loaded into the reconfigurable device. When testing is complete, the testing configuration is erased and the functional blocks may implement other operations. Thus, the set of boundary scan registers consumes no additional chip area. Furthermore, as the set of boundary scan registers disappears after testing, a functional path enabling normal operation modes is unnecessary. Therefore, manually created functional test data is not needed. Instead, ATPG software can create test data from hardware descriptions of the IP core and the set of boundary scan registers.